What is claimed is:

1. A method of forming a semiconductor device in the surface of a substrate, the method comprising the steps of:

separating a semiconductor gate body from the outer surface of the substrate by a gate insulator layer;

forming a conductive drain region in the outer surface of the substrate and spaced apart from the gate body;

forming a conductive source region in the outer surface of the substrate and spaced apart from the gate body opposite the conductive drain region to define a channel region in the substrate disposed inwardly from the gate body and the gate insulator layer;

forming quantum dots on the source region and the drain region;

depositing a metal buffer layer over the conductive source region and conductive drain region;

depositing a metal layer over the metal buffer layer; and

reacting the metal layer and metal buffer layer with the conductive source region and conductive drain region to form respective first and second silicide regions.

2. The method of claim 1, wherein the step of depositing a metal layer over the metal buffer layer includes depositing a metal layer selected from the group consisting of cobalt and nickel.

3. The method of claim 1, wherein the step of reacting the metal layer and metal buffer layer with the conductive source region and conductive drain region includes

annealing the metal layer, metal buffer layer, conductive source region, and conductive drain region.

4. The method of claim 3, wherein the step of annealing includes annealing at a temperature in the range of 450 degrees Centigrade to 850 degrees Centigrade for a time period in the range of 10 seconds to 100 seconds.

5. The method of claim 1, wherein the step of depositing a metal buffer layer further includes depositing a metal buffer layer having a thickness in the range of 1 to 5 nanometers.

6. The method of claim 1, wherein the step of depositing a metal buffer layer over the conductive source region and conductive drain region further includes depositing the metal buffer layer over the gate body and further comprising reacting the metal layer and metal buffer layer with the gate body.

7. The method of claim 1, wherein the step of depositing a metal layer over the metal buffer layer includes depositing a metal layer consisting essentially of cobalt.

8. The method of claim 1, wherein the step of depositing a metal layer over the metal buffer layer includes depositing a metal layer consisting essentially of nickel.

9. A method of forming a semiconductor device in the surface of a substrate, the method comprising the steps of:

separating a semiconductor gate body from the outer surface of the substrate by a gate insulator layer;

forming a conductive drain region in the outer surface of the substrate and spaced apart from the gate body;

forming a conductive source region in the outer surface of the substrate and spaced apart from the gate body opposite the conductive drain region to define a channel region in the substrate disposed inwardly from the gate body and the gate insulator layer;

forming photo resist dots on the source region and the drain region;

etching the photo resist;

depositing a metal buffer layer over the conductive source region and conductive drain region;

depositing a metal layer over the metal buffer layer; and

reacting the metal layer and metal buffer layer with the conductive source region and conductive drain region to form respective first and second silicide regions.

10. The method of claim 1, wherein the step of depositing a metal layer over the metal buffer layer includes depositing a metal layer selected from the group consisting of cobalt and nickel.

11. The method of claim 1, wherein the step of reacting the metal layer and metal buffer layer with the conductive source region and conductive drain region includes annealing the metal layer, metal buffer layer, conductive source region, and conductive drain region.

12. The method of claim 3, wherein the step of annealing includes annealing at a temperature in the range of 450 degrees Centigrade to 850 degrees Centigrade for a time period in the range of 10 seconds to 100 seconds.

13. The method of claim 1, wherein the step of depositing a metal buffer layer further includes depositing a metal buffer layer consisting essentially of zirconium.

14. The method of claim 1, wherein the step of depositing a metal buffer layer further includes depositing a metal buffer layer consisting essentially of hafnium.

15. The method of claim 1, wherein the step of depositing a metal buffer layer further includes depositing a metal buffer layer having a thickness in the range of 1 to 5 nanometers.

16. The method of claim 1, wherein the step of depositing a metal buffer layer over the conductive source region and conductive drain region further includes depositing the metal buffer layer over the gate body and further comprising reacting the metal layer and metal buffer layer with the gate body.

17. The method of claim 1, wherein the step of depositing a metal layer over the metal buffer layer includes depositing a metal layer consisting essentially of cobalt.

18. The method of claim 1, wherein the step of depositing a metal layer over the metal buffer layer includes depositing a metal layer consisting essentially of nickel.